Using the Tektronix Logic Protocol Analyzer

PCI Express is a ubiquitous and flexible bus addressing many markets. Unfortunately this flexibility can also cause integration issues that are very difficult to debug. Rate changes, width changes, spread spectrum clocking and advanced power states can all cause or exacerbate integration bugs. Frequency margining a system is a useful method to ensure that a design will still have margins when it moves to high volume manufacturing. The Tektronix Logic Protocol Analyzer is a valuable tool for tracking and providing visibility of link width changes, rate changes, and advanced power states. Additionally this product family enables the user the flexibility to use spread spectrum clocking and to frequency margin their system while still providing visibility. This paper will present how the Tektronix Logic Protocol Analyzer is used to overcome these challenges using powerful triggering and multiple data views.

Individual Lane Visibility During Link Width Changes

PCI Express busses change their width on the fly for several reasons, most notably to trade off power against bandwidth and to enable high reliability systems by down training link width when a lane fails. This enables the link to maintain operation although at a lower bandwidth. A debug engineer working on a high reliability system will not only need to verify that a width change occurs when a lane fails, but may also need to characterize or optimize how long it takes. The Tektronix Logic Protocol Analyzer allows you to easily trigger on link width changes and view the data on each lane individually and intuitively. Triggering on any link width change is easy: select the Link Event specially designed for this purpose. See Figure 1A.

Clause 1	Add Event Delete Event
	Link Event 🔹 = 🔹 Any Link Width Change 🔹 🖦 On Downstream 🔹 Occurs 💌 🚔 Times
Then	Add Action Delete Action
	Add Clause Delete Clause
	Add State Delete State

Figure 1A. Simple Link Width Change Trigger

Triggering on a specific width change requires a little more effort but is still fairly straightforward; the approach relies on a trigger resource called symbol sequence recognizers. The symbol sequence recognizers can be configured to trigger on any sequence of bytes or symbols on one or more lanes.

To trigger on a specific width change, create a two-state trigger with the symbol sequence recognizers configured for training sequences. The first state looks for a training sequence with the lane number set to 8. The second state looks for a training sequence with the lane number on lane 8 set to PAD. This indicates a link width change from a width of 8 or more to a width of less than 8. Figure 1B shows the two states along with the individual symbol sequence recognizer definitions.



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State 1
Description
Clause 1
If Add Event Delete Event
Sequence V = V Training Sequence Link Number 8 V On Downstream V Lane 8 V Occurs V
Then Add Action Delete Action
Go To
Add Clause Delete Clause
Add State
State 2
Description
Clause 1
Add Event Delete Event
Sequence V = V Training Sequence - Link # Pad V On Downstream V Lane 0 V Occurs V
Then Add Action Delete Action
Trigger All Modules
Add Clause Delete Clause
Add State
Define Symbol Sequence
Name: Training Sequence Link Number 8 Duplicate Name: Training Sequence - Link # Pad Duplicate Duplicate
Length: 16 Remove Save Length: 16 Remove Save
Sym Field NOT Ctl Value Rdy A
0 Comma K COM K28.5 (BC) Sym 0 Comma K COM K28.5 (BC) Sym
1 Link Number X XX Dec ≡ 1 Link Number X XX Dec ≡
2 Lane Number K 08 Hex 2 Lane Number K PAD K23.7 (F7) Sym
3 N_FTS D XXX Dec 3 N_FTS D XX Dec
Data Rate Identifier D X Hex Data Rate Identifier D X Hex
Speed Change [7] X Bin Speed Change [7] X Bin
Auto Chg/De-Emphasis [6] X Bin Auto Chg/De-Emphasis [6] X Bin
4 Reserved [5:3] XXX Bin Generation 2 [2] X Bin Generation 2 [2] X Bin
Add Down Up Delete Add Down Up Delete
Close

Figure 1B. Advanced Link Width Change Trigger



Using the Tektronix Logic Protocol Analyzer

Triggering on the width change is the first requirement; seeing the width change is equally important.

To debug link width changes it is crucial to look at individual bytes on a given lane. Using the LPA's listing window is the most effective tool to display individual bytes on each and every lane. However, width change can potentially take many milliseconds to complete and this can result in pages and pages of listing window data

What is needed is a way to see a high level view of the width change and then easily drill down into the lane by lane, byte by byte information.

TLA Timestamp		Link	PacketTy	/pe		STP	
4856:916:172	+	SA 1	UpdateFG	-P			
4856:916:187	+	6:916:1728A1 SA 1	UpdateFC	-NP			
	18	6917190882 6917:4618A1					
4856-941-688		SA 2	TS1 (15)	Width	Data Ra	te	
100013 121000	Li	nk #0		x8	2.5		
4856:941:850		SA 1	TS1 (22)	Width	Data Ra	te	
	Li	nk #0		x8	2.5/5.0)	
4856:942:712		SA 2	TS2 (33)	Width	Data Ra	te	
100017 1217 12	Li	nk #0		x8	2.5		
4856-943-319		SA 1	TS2 (23)	Width	Data Ra	te	
100013 101013	Li	nk #0		x8	2.5/5.0)	
4856-046-131		SA 1	TS1 (33380) Width	Vidth Data R		
4850.940.151	Li	nk #0		Changin	g 2.5/5	5.0	
4856-046-376		SA 2	TS1 (31161) Width	Width Data R		
4050.540.570	Li	nk #247		Changin	g 2.5	;	
	48	58:946:457 8A 2 58:946:476 8A 2			-	_	
4859:088:339		SA 2	TS1 (86)	Width	Data R	ate	
	Li	nk #?		NotAligned	2.5		
	488	59:088:652 SA 1 59:093:908 SA 2 59:093:973 SA 2					
4950-207-769		SA 2	TS1 (7)	Width	Data Ra	te	
4859:507:708	Li	nk #0		Changing	2.5		
4950-209-010		SA 1	TS1 (6)	Width	Data Ra	te	
4859:508:019	Li	nk #0		Changing	2.5/5.0) (
4950,209,279		SA 2	TS1 (6)	Width	Data Ra	te	
4839.308.278	Li	nk #0		x16	2.5		
4950,209,494		SA 1	TS1 (7)	Width	Data Ra	te	
+659:506:+64	Li	nk #0		x16	2.5/5.0)	
4950,209,742		SA 2	TS2 (23)	Width	Data Ra	ite	
4059:508:745	Li	nk #0		x16	2.5		
4950,309-009		SA 1	TS2 (18)	Width	Data Ra	te	
4059:308:998	Li	nk #0		x16	2.5/5.0)	
4859:310:438	+	SA 2	InitFC1-P				

Figure 2A. Transaction Window Width Change

The LPA transaction window provides the high level view allowing a user to see the entire width change on one screen; the listing window allows a user to drill down into individual training sequences of interest. Co-scrolling the two windows together makes it easy to keep track of the details within the high level view.

The transaction window capture of a x8 to x16 width change shown in Figure 2A, spans about 2.4ms. By filtering and collapsing repetitive ordered sets the user can see the entire width change. When the width change functions correctly, the display provides the necessary information, and the user can move on. For the high reliability system described at the beginning of this section the transaction window quickly shows how long the width change takes and some possibilities for optimization.



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Timestamp	Uni_Up Link Details	Uni_Up UpO	Uni_Up Up1	Uni_Up Up2	Uni_Up Up3	Uni_Up Up4	Uni_Up Up5	Uni_Up Up6	Uni_Up Up7
-2.148,892,375 ms	**** TS1 - Not Aligned *******************	COM	COM	COM	COM	No_Sig	No_DL>	No_Sia	No_Sig
-2.148,876,446 ms	Link No: Unknown (Not Aligned)	PAD	PAD	PAD	PAD	No_DL>	No_DL>	No_DL>	No_DL>
-2.148,875,509 ms	Lane Ordering: Unknown (Not Aligned)	PAD	PAD	PAD	PAD	No_DL>	No_DL>	No_DL>	No_DL>
-2.148,874,572 ms	N_FTS: 24 Dec	18	18	18	18	No_DL>	No_SL>	No_DL>	No_DL>
-2.148,873,635 ms	Data Rate ID: 06 Hex	06	06	06	06	No_DL>	No_SL>	No_DL>	No_DL>
	Gen 2 rate supported								
1	Gen 1 rate supported								
-2.148,861,454 ms	Training Control: 00 Hex	00	00	00	00	No_SL>	COM	No_SL>	No_SL>
1	Hot Reset: De-assert								
1	Disable Link: De-assert								
1	Loopback: De-assert								
1	Disable Scrambling: De-assert								
	Compliance Receive: De-assert								
-2.148,860,517 ms	TS1 Identifier	4A	4A	4A	4A	No_SL>	B5	No_SL>	No_SL>
-2.148,859,580 ms	TS1 Identifier	4A	4A	4A	4A	No_SL>	85	No_SL>	No_SL>
-2.148,858,643 ms	ISI Identifier	4A	44	44	4A	NO_SL>	85	NO_SL>	NO_SL>
-2.148,842,/14 ms	ISI Identifier	4A	44	44	44	NO_SL>	85	NO_SL>	NO_SL>
-2.148,841,/// ms	TS1 Identifier	44	44	4A	44	NO_SL>	85	NO_SL>	NO_SL>
-2.148,840,840 ms	TS1 Identifier	44	44	4A	44	NO_SL>	85	NO_SL>	NO_SL>
-2.148,839,903 ms	TS1 Identifier	44	44	44	44	NO_SL>	65	NO_SL>	NO_SL>
-2.148,827,722 ms	TSL Identifier	44	44	44	44	NO_SL>	65	NO_SL>	NO_SL>
-2.148,826,785 ms	TSI Identifien	140	44	44	44	NO_SL>	65	NO_SL>	NO_SL>
-2.140,025,040 ms	Size TS1 - Not Aligned Sectorescenters	COM	CON	CON	CON		K2R C		
-2.140,024,511 ms	Link Net Unknown (Net Aligned)	RAD	RAD	RAD	RAD	KOM C	RAD	COM	COM
-2.148,012,730 ms	Lane Ordening: Unknown (Not Aligned)	PAD	PAD	PAD	PAD	PAD	18	PAD	PAD
-2.148 810 856 ms	N FTS: 24 Dec	18	18	18	18	18	106	18	18
-2.148 809 919 ms	Data Rate ID: 06 Hex	06	06	06	06	06	00	06	06
2.140,005,515 ms	Gen 2 rate supported								
1	Gen 1 rate supported								
-2.148.793.990 ms	Training Control: 00 Hex	00	00	00	00	00	AD	00	00
	Hot Reset: De-assert								
1	Disable Link: De-assert								
1	Loopback: De-assert								
1	Disable Scrambling: De-assert								
1	Compliance Receive: De-assert								
-2.148,793,053 ms	TS1 Identifier	4A	4A	4A	4A	4A	48	4A	4A
-2.148,792,116 ms	TS1 Identifier	4A	4A	4A	4A	4A	C8	4A	4A
-2.148,791,179 ms	TS1 Identifier	4A	4A	4A	4A	4A	38	4A	4A
-2.148,778,998 ms	TS1 Identifier	4A	4A	4A	4A	4A	24	4A	4A
-2.148,778,061 ms	TS1 Identifier	4A	4A	4A	4A	4A	62	4A	4A
-2.148,777,124 ms	TS1 Identifier	4A	4A	4A	4A	4A	EC	4A	4A
-2.148,776,187 ms	TS1 Identifier	4A	4A	4A	4A	4A	F4	4A	4A
-2.148,764,006 ms	TS1 Identifier	4A	4A	4A	4A	4A	27	4A	4A
-2.148,763,069 ms	TS1 Identifier	4A	4A	4A	4A	4A	F5	4A	4A
-2.148,762,132 ms	TS1 Identifier	4A	4A	4A	4A	4A	COM	4A	4A
-2.148,761,195 ms	Not Aligned	COM	COM	COM	COM	COM	K28.6	COM	COM
-2.148,749,014 ms	Not Aligned	PAD	PAD	PAD	PAD	K28.6	PAD	K28.6	K28.6
-2.148,748,077 ms	Not Aligned	PAD	PAD	PAD	PAD	PAD	08	PAD	PAD
-2.148,747,140 ms	Not Aligned	18	18	18	18	18	12	18	18
-2.148,746,203 ms	Not Aligned	06	06	06	06	06	62	06	06
-2.148,/30,2/4 ms	Not Aligned	00	00	00	00	00	40	00	00
-2.148,/29,33/ MS	Not Aligned	44	44	44	44	44	48	44	44
-2.148,728,400 MS	Not Aligned	44	44	44	44	44	20	44	44
-2.148,/2/,463 MS	Not Aligned	44	44	44	44	44	38	44	44
-2.140,715,282 MS	Not Aligned	170	44	44	44	44	63	140	44
-2.140,/14,345 MS	Not Aligned	44	44	44	44	44	26	40	44
-2.140,/12,4/1 MS	Not Aligned	44	44	44	44	44	EC E4	44	44
-2.148,700,250 MS	Not Aligned	44	44	44	44	44	27	44	44
-2.140,035,333 MS	Not Aligned	44	44	44	44	44	ÉS	COM	44
2.140,030,410 MS	Inversityred	10	10	10	10	-10	1.02	COM	10

Figure 2B. Listing Window Width Change

If something interesting did occur and some of the ordered sets need to be analyzed in more detail, then the listing window shown in Figure 2B, provides decoded lane level data. By "locking" the transaction to the listing window, the user can quickly navigate to an area of interest using the transaction window and the system will display the details of the item in the listing window.

Rate Change Capture

The PCI Express specification allows two agents to negotiate speed on the fly. Providing visibility of these successful or unsuccessful speed changes is a strength of the Logic Protocol Analyzer. As with width changes, debug starts with powerful and easy to use triggering capabilities. A user can either trigger on a successful speed change with a simple trigger or the user can use symbol sequence recognizers to trigger on training sequences with the speed change bit asserted as part of a trigger.



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Clause 1	Add Event Delete Event		
	Link Event 💌 = 💌 Any Data Rate Change	▼ On Downstream ▼ Occurs	•
Then	Add Action Delete Action		
	Trigger All Modules 🔹		

Figure 3A. Simple Rate Change Trigger

State 1	A user can also define a trigger to look for failed rate changes, one example of which is shown in Figure 3B.
Description	The trigger uses the rate change link event trigger shown above combined with a timer and a symbol sequence
Clause 1	recognizer. This kind of trigger is very powerful when use
If Add Event Delete Event	that occur infrequently.
Sequence 🗨 = 💌 TS1 - Speed Change	This particular trigger is a simple example using symbol
Then Aller Ditter	 sequence recognizers. Combining packet or ordered set triggers with multiple states, counters, and timers lets the
Men Add Action Delete Action	user find a variety of complex issues inlcuding missed
Reset and Start Timer	LTSSM transitions and timeouts among many others.
And Go To 💌 State 2 💌	
Description	
Clause 1	
Clause 1 If Add Event Delete Event	
Clause 1 If Add Event Delete Event Link Event = Any Data Rate Change	
Clause 1 If Add Event Delete Event Link Event Event Any Data Rate Change	
Clause 1 If Add Event Delete Event Link Event = Any Data Rate Change Then Add Action Delete Action	
Clause 1 If Add Event Delete Event Link Event = Any Data Rate Change Then Add Action Delete Action Go To State 1	
Clause 1 If Add Event Delete Event Link Event = Any Data Rate Change Then Add Action Delete Action Go To State 1	
Clause 1 If Add Event Delete Event Link Event = Any Data Rate Change Then Add Action Delete Action Go To State 1	
Clause 1	
Clause 1 If Add Event Delete Event Link Event Any Data Rate Change Then Add Action Delete Action Go To State 1 Clause 2 Else If Add Event Delete Event	
Clause 1 If Add Event Delete Event Link Event	
Clause 1 If Add Event Delete Event Link Event = Any Data Rate Change Then Add Action Delete Action Go To State 1 Clause 2 Else If Add Event Delete Event Timer 1 Zms Then Add Action Delete Action	
Clause 1 Image: Image: Ima	

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TLA Timestamp		Link		Pac	ketType			
046:501:230	+	UpStream		Upd	ateFC-P			
	_	046:505:5891 046:506:33	ownStream 4 UpStream					
046+510+142	D	ownStream	TS1 (15)	Width	Da	ta Rate	
040.315.142	Li	nk #0			x16	2	.5/5.0	
046-510-204	l	JpStream	TS1 (22))	Width		ta Rate	Í
040:519:294	Li	nk #0			x16		2.5/5.0	
046-520-167	D	ownStream	T52 (34)	Width		ta Rate	
046:520:167	Li	nk #0			x16		.5/5.0	
046-520-767	l	JpStream	TS2 (23))	Width	Da	ta Rate	Í
046:520:767	Li	nk #0			x16	2	.5/5.0	
046-522-540		DownStreet	ownShoom	Lind	atoEC-ND			
040:522:549	+	DownStrea	111	opu	ateronip			
046:522:551	+	DownStrea	am	Upd	ateFC-P			
046:522:602	+	UpStream		Upd	ateFC-P			
046-522-602	l	JpStream	TS1 (1	.9)	Width		Data Rat	
046:522:603	Li	nk #0	Speed C	hange	e x	16	0	
046-500-770	D	ownStream	TS1 (7)		Width	Da)ata Rate	
046:522:772	Li	nk #0			x16	2	2.5/5.0	
	D	ownStream	TS1 (7)	Widt	1	Data Ra	ate
046:523:286	Li	nk #0	Speed C	hange	e)	(16	2.5/5.	0
	D	ownStream	TS2 (4	1 1)	Widt	h Data		ate
046:523:799	Li	nk #0	Speed C	hange	e)	(16	2.5/5.	0
046.555.054	l	JpStream	TS2 (3	8)	Width	1	Data Ra	ate
046:523:901	Li	nk #0	Speed C	hange	e x	16	2.5/5.0	0
		046.526.3 046.526.4	9 UpStream 4 UpStream		•			
		046:526:4850 046:526:5000	ownStream		Width		ata Data	5
046:527:516		ownstream	151 (15	/		10	ala Kate Dic/cio	
		IK # !	TC1 (00)	N	ot Alighed		2.3/5.0	Ļ
046:527:600		up stream	151 (22)	/	width		ata Kate	1
	Li	NK #?	ownStream	N	ot Aligned		2.5/5.0	
046-500.064	D	ownStream	T52 (34)	Width	Da	ta Rate	Ì
046:528:061	Li	nk #0			x16	2	.5/5.0	
	_	046/628/33	SUISHOOM			Data Rate		
		InStream	TS2 (22)		Width	Da	ta Rate	

As with the width change example above, triggering on an event is the first requirement; seeing the data is equally important both at the highest level and at the lowest lane by lane level.

For many speed change issues, the transaction window shown in Figure 4 displays the level of detail needed to see the entire speed change. There are some problems (such as a failed speed change) that require lane level visibility and are better viewed in the listing window.

The complexities of link equalization negotiation introduced into PCIE 3.0 increases the relevance of lane elements such as preset hints. Actual cursor settings on each lane become critical pieces of information. Below is shown the listing window view of the link equalization transitioning from Phase 1 to Phase 2.

If the system under test is failing the rate change to 8Gb/s due to the equalization negotiation, a user may need to cross trigger an oscilloscope and verify the equalization settings are actually being applied.

Figure 4. Complete Rate Change in Transaction Window

24020-162-024	P4 Tx	TS1	Width	Data Rate	EQ Cont	EQ Preset	(dB)
24930:162:924	Link #0		Changing	2.5/5.0/8.0	Phase 0	0	0
24020-462-020	P4 Tx	TS1	Width	Data Rate	EQ Cont	EQ Preset	(dB)
24930:162:939	Link #0		x16	2.5/5.0/8.0	Phase 0	0	0

TLA Timestamp	Link P	acketType	STP_Seq	lum Fmt	TC TD	TH E	P At	ttr Length	HdrFC	: Da	taFC V	C ID A	kNak_Se	eqNum				
005:362:769	SA 1_Up	TS1 (795)	Width	Data Rate	EQ Cont	EQ Preset	(dB)	EQ (Pre / Post	dB) Lr	n OLI	n1 Ln2	2 Ln 3	Ln 4	Ln 5 Li	n6 Ln7]		
00010021703	Link #2		x8	2.5/5.0/8.0	Phase 2	0	0		0/	0-5	.7/0 -0.3/	-0.3 -1.2	0 -0.6/0	0/-0.3 0/	0 0/-1.5	·····		
005:365:14	7 5A 1_6h		are bit				(15)	50 (0 (0)	10)							7		
005:365:162	SA 1_Dn	151 (658)	width	Data Rate	EQ Cont	EQ Preset	(dB)	EQ (Pre/Post	ab) Li	nu Li	n 1 Ln 2	2 Ln a	5 Ln 4	Ln 5 Li	n 6 Ln /			
00010001102	Link #2		x8	2.5/5.0/8.0	Phase 2	0	0		0/0	0 -5	.7/0 -0.3/	-0.3 -1.2	0 -0.6/0	0/-0.3 0/	0 0/-1.5			
005-076-140	SA 1_Up	TS1 (9)	Width	Data Rate	EQ Cont	EQ Preset	(dB)	EQ (Pre / Post	dB) Lr	n 0	Ln 1	Ln 2	Ln 3	Ln 4	Ln 5	Ln 6	Ln 7	ר
005:576:149	Link #2		x 8	2.5/5.0/8.0	Phase 3	0	0		-4	.2/-4.7	-4.2/-4.7	-4.2/-4.7	-4.2/-4.7	7 -4.2/-4.7	7 -4.2/-4.7	-4.2/-4.7	-4.2/-4.7	
005-076-004	SA 1_Dn	TS1 (736)	Width	Data Rate	EQ Cont	EQ Preset	(dB)	EQ (Pre / Post	dB) Lr	n 0	Ln 1	Ln 2	Ln 3	Ln 4	Ln 5	Ln 6	Ln 7	ī
005:376:224	Link #2		x 8	2.5/5.0/8.0	Phase 3	-2.5	0		-4	.2/-4.7	-4.2/-4.7	-4.2/-4.7	-4.2/-4.7	7 -4.2/-4.7	7 -4.2/-4.7	-4.2/-4.7	-4.2/-4.7	
005-076-010	SA 1_Up	TS1 (736)	Width	Data Rate	EQ Cont	EQ Preset	(dB)	EQ (Pre / Post	dB) Lr	n 0	Ln 1	Ln 2	Ln 3	Ln 4	Ln 5	Ln 6	Ln 7	ר
005:376:310	Link #2		x 8	2.5/5.0/8.0	Phase 3	-2.5	0		-4	.2/-4.7	-4.2/-4.7	-4.2/-4.7	-4.2/-4.7	7 -4.2/-4.7	7 -4.2/-4.7	-4.2/-4.7	-4.2/-4.7	
005-000-000	SA 1_Dn	TS1 (9189)	Width	Data Rate	EQ Cont	EQ Prese	t (dB)	EQ (Pre / Post	:dB) L	.n 0	Ln 1	Ln 2	Ln 3	Ln 4	Ln 5	Ln 6	Ln 7	Г
005:388:606	Link #2		x8	2.5/5.0/8.0	Phase 3	-2.5	0		-3	6.6/-4	-4.2/-4.7	-4.2/-4.7	-4.2/-4.7	-4.1/-4.1	-4.2/-4.7	-4.2/-4.7	-4.1/-4.1	
005-000-000	SA 1_Up	TS1 (9190)	Width	Data Rate	EQ Cont	EQ Prese	t (dB)	EQ (Pre / Post	:dB) L	.n 0	Ln 1	Ln 2	Ln 3	Ln 4	Ln 5	Ln 6	Ln 7	Í
005:388:693	Link #2		x8	2.5/5.0/8.0	Phase 3	-2.5	0		-3	6/-4	-4.2/-4.7	-4.2/-4.7	-4.2/-4.7	-4.1/-4.1	-4.2/-4.7	-4.2/-4.7	-4.1/-4.1	



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Case TSL Construction Desc Desc <thdesc< th=""> Desc <thdesc< th=""></thdesc<></thdesc<>	Uni_Dn Link Details	Uni_ DnO	Uni_ Dr1	Uni_ Dn2	Uni Dn3
Link No: 0 Dec 00	TC1	110	110	110	1.0
Lane Ordering: 00 <td>Link No: 0 Dec</td> <td>00</td> <td>00</td> <td>00</td> <td>00</td>	Link No: 0 Dec	00	00	00	00
12:3:4:4:5:6,7:8:9:10.11.12.13.14.15 00 01 02 02 N_FTS: 94 Dec 5E 5E 5E 5E 5E Data Rate ID: 0E Hex 0E 0E 0E 0E 0E Gen 3 rate supported	Lane Ordening:	00	01	02	03
N_FTS: 94 Dec SE SE <td></td> <td></td> <td></td> <td></td> <td></td>					
Data Rate ID: OC 0E 0E<	N FTS: 94 Dec	SE	SE	SE	SE
Gen 3 rate supported	Data Rate ID: OF Hex	0F	OF	OF	OF
Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex 00 00 00 00 Hot Reset: De-assert Disable Link: De-assert Compliance Receive: De-assert EQUISI: 39 Hex 39 39 39 39 39 39 Equalization Control: 01b Trainsmitter Preset: 011b FS: 3E Hex 15 <t< td=""><td>Gen 3 rate supported</td><td></td><td></td><td></td><td></td></t<>	Gen 3 rate supported				
Gen 1 rate supported Training Control: 00 Hex 00 00 00 00 Hot Reset: De-assert Disable Link: De-assert Compliance Receive: De-assert Compliance Receive: De-assert Compliance Receive: De-assert Compliance Receive: De-assert Compliance Receive: De-assert Transmitter Preset: 011b Si Edwalting: De-assert <td>Gen 2 rate supported</td> <td></td> <td></td> <td></td> <td></td>	Gen 2 rate supported				
Training Control: 00 Hex 00 00 00 00 00 Hot Reset: De-assert	Gen 1 rate supported				
Hot Reset: De-assert	Training Control: 00 Hex	00	00	00	00
Disable Link: De-assert	Hot Reset: De-assert				
Loopback: De-assert	Disable Link: De-assert				
Disable Scrambling: De-assert	Loopback: De-assert				
Compliance Receive: De-assert	Disable Scrambling: De-assert				
EQ TS1: 39 Hex Equalization Control: 01b Reset EIEOS Interval: De-assert Transmitter Preset: 0111b Use Preset: De-assert F5: 3E Hex LF: 15 Hex TSL Q Control: 8D Hex Post-Cursor Coefficient: 0D Hex Reject Coefficient Values: De-assert TS1 Identifier TS1 Det Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Compliance Receive: De-assert Transmitter Preset: 0111b Transmitter Preset: 011b Transmitter Preset: 014 TSI Identifier TSI	Compliance Receive: De-assert				
Equalization Control: 01b	EQ TS1: 39 Hex	39	39	39	39
Reset EIEOS Interval: De-assert	Equalization Control: 01b				
Transmitter Preset: 0111b	Reset EIEOS Interval: De-assert				
Use Preset: De-assert FS: 3E Hex 3E 3E 3E 3E 3E LF: 15 Hex 15 15 15 15 15 TS1 EQ Control: 8D Hex 8D 8D 8D 8D 8D 8D Post-Cursor Coefficient: 0D Hex Parity: Assert TS1 Identifier 4A 4A 4A 4A 4A 4A 4A TS1 Identifier 00 00 00 00 00 <td>Transmitter Preset: 0111b</td> <td></td> <td></td> <td></td> <td></td>	Transmitter Preset: 0111b				
FS: 3E Hex 3E	Use Preset: De-assert				
LF: 15 Hex TSI EQ Control: 8D Hex Reject Coefficient: 0D Hex Reject Coefficient Values: De-assert Parity: Assert TSI Identifier TSI Det Coefficient: 0D Hex N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Disable Scrambling: De-assert Compliance Receive: De-assert Transmitter Preset: 011b Use Preset: De-assert Transmitter Preset: 011b Use Preset: De-assert Pre-Cursor Coefficient: 0B Hex Reject Coefficient: 0B Hex Post-Cursor Coefficient: 0D Hex Reject Coefficient: 2B Hex TSI Identifier AA 4A 4A TSI Identifier AA 3A 3A AA 3A AA 3A AA 3A AA 3A AA 3A AA 3A AA 4A 4A AA 4A	FS: 3E Hex	3E	3E	3E	3E
TS1 EQ Control: 8D Hex Post-Cursor Coefficient: 0D Hex Reject Coefficient Values: De-assert Parity: Assert 8D 8D 8D 8D 8D Parity: Assert TS1 Identifier 4A 4A 4A 4A 4A 4A 4A TS1 Identifier 08 08 80 80 80 80 TS1 Identifier 4A 4A 4A 4A 4A 4A 4A TS1 Identifier 00 00	LF: 15 Hex	15	15	15	15
Post-Cursor Coefficient: 0D Hex Reject Coefficient Values: De-assert Parity: AssertTSI Identifier4A4A4A4ATSI Identifier4A4A4A4ATSI Identifier4A4A4A4ATSI Identifier4A4A4A4ATSI Identifier4A4A4A4ATSI Identifier4A4A4A4ATSI Identifier4A4A4A4ATSI Identifier00000000Lane Ordering:000000000,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15SESESEN_FTS: 94 Dec00000000Gen 1 rate supportedGen 2 rate supportedTraining Control: 00 Hex000000Hot Reset: De-assertDisable Link: De-assertCompliance Receive: De-assertReset EIEOS Interval: De-assertTransmitter Preset: 011bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex060606Cursor Coefficient: 06 Hex060606Cursor Coefficient: 28 Hex282828SI Identifier	TS1 EQ Control: 8D Hex	8D	8D	8D	8D
Reject Coefficient Values: De-assertParity: AssertTSI Identifier4A4A4A4A4ATSI Identifier4A4A4A4A4ATSI Identifier4A4A4A4A4ATSI Identifier4A4A4A4A4ADE Balance0808080804TSI Identifier0000000000Link No: 0 Dec00000000Lane Ordering:000000000,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15N_FTS: 94 Dec0E0E0E0EData Rate ID: 0E Hex00000000Gen 1 rate supportedTraining Control: 00 Hex00000000Hot Reset: De-assertDisable Link: De-assertCompliance Receive: De-assertCompliance Receive: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertDisable Scrambling: De-assertDisable Scrambling: De-assertDisable Scrambling: De-assert <td>Post-Cursor Coefficient: OD Hex</td> <td></td> <td></td> <td></td> <td></td>	Post-Cursor Coefficient: OD Hex				
Parity: Assert	Reject Coefficient Values: De-assert				
TS1 Identifier4A4A4A4ATS1 Indentifier4A4A4A4ATs1 Identifier4A4A4A4ATs1 Identifier4A4A4ATs1 Identifier4A4A4A4ATs1 Identifier4A4A4A4ATs1 Identifier4A4A4A4ATs1 Identifier4A4A4A4ATs1 Identifier4A4A4A4ATs1 Identifier4A4A4A4A<	Parity: Assert				
TS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4A4ATS1 Identifier4A4A4A4A4ADC Balance0808080808TS1 TS1 TS1 TS1 TS1 TS1TS1 TS1 TS1TS1 TS1 TS1TS1 TS1 TS1TS1 TS1 TS1Link No: 0 Dec0000000000Link No: 0 Dec00000102030,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15N_FTS: 94 Dec5E5E5E5E5EData Rate ID: 0E Hex0E0E0E0EGen 1 rate supportedGen 1 rate supportedTraining Control: 00 Hex00000000Hot Reset: De-assertDisable Link: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertTransmitter Preset: 011bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex060606Cursor Coefficient: 28 Hex282828TSI Identifier4A4A4ATSI Identifier4A4A4ATSI Identifier4A4A4ATSI Identifier4A4A4ATSI Identifier <t< td=""><td>TS1 Identifier</td><td>4A</td><td>4A</td><td>4A</td><td>4A</td></t<>	TS1 Identifier	4A	4A	4A	4A
TS1 Identifier 4A 4A 4A 4A 4A TS1 Identifier 4A 4A 4A 4A TS1 Identifier 4A 4A 4A 4A TS1 Identifier 00 00 00 00 00 Identifier 4A 4A 4A 4A 4A Identifier 4A 4A 4A 4A Identifier 4A 4A 4A 4A Identifier <td>TS1 Identifier</td> <td>4A</td> <td>4A</td> <td>4A</td> <td>4A</td>	TS1 Identifier	4A	4A	4A	4A
TS1 Identifier 4A 4A 4A 4A 4A TS1 Identifier 4A 4A 4A 4A 4A DC Balance 08 08 08 08 TS1 TS1 TS1 TS1 TS1 TS1 Link No: 0 Dec 00 00 00 00 00 Lare Ordering: 00 00 01 02 03 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec DE 0E 1DE 1	TS1 Identifier	4A	4A	4A	4A
TS1 Identifier 4A 4A 4A 4A 4A DC Balance 08 08 08 4A DC Balance 00 00 00 00 00 Link No: 0 Dec 00 00 00 00 00 00 Link No: 0 Dec 00 01 02 03 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 <td< td=""><td>TC1 Tda atifica</td><td>4.4</td><td>4.4</td><td>4.4</td><td>4.4</td></td<>	TC1 Tda atifica	4.4	4.4	4.4	4.4
DC Balance 08 08 08 08 08 44 TS1 TS1 <thts1< th=""> TS1 <thts1< th=""></thts1<></thts1<>	ISI Identifier	4A	4A	4A	4A
TS1 ************************************	TS1 Identifier	4A 4A	4A 4A	4A 4A	4A 4A
Link No: 0 Dec 00 <td>TS1 Identifier DC Balance</td> <td>4A 4A 08</td> <td>4A 4A 08</td> <td>4A 4A 08</td> <td>4A 4A 4A</td>	TS1 Identifier DC Balance	4A 4A 08	4A 4A 08	4A 4A 08	4A 4A 4A
Lane Ordering: 00 01 02 03 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15	TS1 Identifier DC Balance	4A 4A 08 1E	4A 4A 08 1E	4A 4A 08 1E	4A 4A 4A 1E
0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15	TS1 Identifier DC Balance **** TS1 *******************************	4A 08 1E 00	4A 4A 08 1E 00	4A 08 1E 00	4A 4A 4A 1E 00
N_FTS: 94 DecSESESESESESEData Rate ID: 0E Hex0E0E0E0E0E0EGen 3 rate supportedGen 1 rate supportedTraining Control: 00 Hex0000000000Hot Reset: De-assertDisable Link: De-assertLoopback: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertEQ TS1: 3A Hex3A3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertVse Preset: De-assertVse Preset: De-assertVse Preset: De-assertPre-Cursor Coefficient: 0B Hex06060606Cursor Coefficient Values: De-assertParity: AssertTS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A <td>TSI Identifier DC Balance TSI ************************************</td> <td>4A 08 1E 00 00</td> <td>4A 08 1E 00 01</td> <td>4A 08 1E 00 02</td> <td>4A 4A 1E 00 03</td>	TSI Identifier DC Balance TSI ************************************	4A 08 1E 00 00	4A 08 1E 00 01	4A 08 1E 00 02	4A 4A 1E 00 03
Data Rate ID: OE HexOEOEOEOEOEOEGen 3 rate supportedGen 1 rate supportedTraining Control: OO HexOOOOOOOOHot Reset: De-assertDisable Link: De-assertLoopback: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex060606Cursor Coefficient: 28 Hex282828TS1 EQ Control: 8D Hex8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4ATS1 Identifier4A4ATS1 Identifier4A4ATS1 Identifier4A4ATS1 Identifier4A4ATS1 Identifier4A4ATS1 Identifier4A4ATS1 Identifier4A4ATS1 Identifier4A4ATS1 Identifier4A4ATS	TS1 Identifier TS1 Identifier DC Balance TS1 Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15	4A 08 1E 00 00	4A 4A 08 1E 00 01	4A 08 1E 00 02	4A 4A 1E 00 03
Gen 3 rate supportedGen 1 rate supportedTraining Control: 00 Hex00000000Hot Reset: De-assertDisable Link: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertEQ TS1: 3A Hex3A3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex060606Cursor Coefficient: 2B Hex2B2B2BParity: AssertParity: AssertTS1 Identifier4A4A4ATS1 Identifier4A4A4A	TS1 Identifier TS1 Identifier DC Balance TS1 Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec	4A 08 1E 00 00 5E	4A 08 1E 00 01 5E	4A 08 1E 00 02 5E	4A 4A 1E 00 03 5E
Gen 2 rate supportedGen 1 rate supportedTraining Control: 00 Hex00000000Hot Reset: De-assertDisable Link: De-assertLoopback: De-assertDisable Scrambling: De-assertEQ TS1: 3A Hex3A3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex06060606Cursor Coefficient: 28 Hex28282828TS1 EQ Control: 8D HexParity: AssertTS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier	TS1 Identifier DC Balance TS1 ************************************	4A 08 1E 00 00 5E 0E	4A 08 1E 00 01 5E 0E	4A 08 1E 00 02 5E 0E	4A 4A 4A 00 03 5E 0E
Gen 1 rate supportedTraining Control: 00 Hex00000000Hot Reset: De-assertDisable Link: De-assertLoopback: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertEQ TS1: 3A Hex3A3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex060606Cursor Coefficient: 28 Hex28282828TS1 EQ Control: 8D Hex8D8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4A </td <td>TSI Identifier TSI Identifier DC Balance TSI Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported</td> <td>4A 08 00 00 5E 0E</td> <td>4A 4A 08 00 01 5E 0E </td> <td>4A 08 00 02 5E 0E</td> <td>4A 4A 4A 00 03 5E 0E </td>	TSI Identifier TSI Identifier DC Balance TSI Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported	4A 08 00 00 5E 0E	4A 4A 08 00 01 5E 0E 	4A 08 00 02 5E 0E	4A 4A 4A 00 03 5E 0E
Training Control: 00 Hex00000000Hot Reset: De-assertDisable Link: De-assertLoopback: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertEQ TS1: 3A Hex3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex060606Cursor Coefficient: 2B Hex2B2B2BTS1 EQ Control: 8D Hex8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4ATS1 Identifier4A <td< td=""><td>TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 2 rate supported</td><td>4A 08 1E 00 00 5E 0E </td><td>4A 4A 08 1E 00 01 5E 0E </td><td>4A 08 1E 00 02 5E 0E </td><td>4A 4A 4A 00 03 5E 0E </td></td<>	TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 2 rate supported	4A 08 1E 00 00 5E 0E 	4A 4A 08 1E 00 01 5E 0E 	4A 08 1E 00 02 5E 0E 	4A 4A 4A 00 03 5E 0E
Hot Reset: De-assertDisable Link: De-assertLoopback: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertEQ TS1: 3A Hex3A3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex06060606Cursor Coefficient: 2B Hex2B2B2B2BTS1 EQ Control: 8D Hex8D8D8D8D8DPost-Cursor Coefficient: 0D HexTS1 Identifier4A4A4A4ATS1 Id	TSI Identifier DC Balance TSI ************************************	4A 08 1E 00 00 5E 0E	4A 08 1E 00 01 5E 0E	4A 08 1E 00 02 5E 0E 	4A 4A 4A 00 03 5E 0E
Disable Link: De-assertLoopback: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertEQ TS1: 3A Hex3A3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex06060606Cursor Coefficient: 2B Hex2B2B2B2BTS1 EQ Control: 8D Hex8D8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4A4ATS1 I	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 2 rate supported Gen 1 rate supported Training Control: 00 Hex	4A 08 00 00 5E 0E 00	4A 08 1E 00 01 5E 0E 00	4A 08 1E 00 02 5E 0E 00	4A 4A 4A 00 03 5E 0E 00
Loopback: De-assertDisable Scrambling: De-assertCompliance Receive: De-assertEQ TS1: 3A Hex3A3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex06060606Cursor Coefficient: 2B Hex2B2B2B2BTS1 EQ Control: 8D Hex8D8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4A4ATS1 Identifier4A <td>TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Distance decided and and and and and and and and and an</td> <td>4A 08 00 00 5E 0E 00</td> <td>4A 08 00 01 5E 0E 00</td> <td>4A 08 1E 00 02 5E 0E 00 </td> <td>4A 4A 4A 00 03 5E 0E 00 </td>	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Distance decided and and and and and and and and and an	4A 08 00 00 5E 0E 00	4A 08 00 01 5E 0E 00	4A 08 1E 00 02 5E 0E 00 	4A 4A 4A 00 03 5E 0E 00
Disable Scrambling: De-assertCompliance Receive: De-assertEQ TS1: 3A Hex3A3A3A3AEqualization Control: 10bReset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex06060606Cursor Coefficient: 2B Hex2B2B2B2BTS1 EQ Control: 8D Hex8D8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4A4ATS1 Identifier4A4A4A </td <td>TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert</td> <td>4A 08 1E 00 00 00 5E 0E 00</td> <td>4A 08 00 01 5E 0E 00 </td> <td>4A 08 1E 00 02 5E 0E 00 </td> <td>4A 4A 4A 00 03 5E 0E 00 00 </td>	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lane Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert	4A 08 1E 00 00 00 5E 0E 00	4A 08 00 01 5E 0E 00 	4A 08 1E 00 02 5E 0E 00 	4A 4A 4A 00 03 5E 0E 00 00
EQ TS1: 3A Hex3A3A3AEqualization Control: 10b	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Disable Link: De-assert Disable Link: De-assert	4A 08 1E 00 00 00 00 00 00 00 00 00 00 00 00 00	4A 08 1E 00 01 5E 0E 00 00	4A 08 1E 00 02 5E 0E 00 00	4A 4A 4A 00 03 5E 0E 00
EQUISE: 3A Hex3A3A3A3AEqualization Control: 10bReset ELEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex060606Cursor Coefficient: 28 Hex282828TS1 EQ Control: 8D Hex8D8D8DPost-Cursor Coefficient: 0D HexParity: AssertTS1 Identifier4A4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Loopback: De-assert Disable Scrambling: De-assert	4A 08 1E 00 00 5E 0E 00 	4A 08 1E 00 01 5E 0E 00 00 	4A 08 1E 00 02 5E 0E 00 	4A 4A 4A 00 03 5E 0E 00
Equalization Control: 100Reset EIEOS Interval: De-assertTransmitter Preset: 0111bUse Preset: De-assertPre-Cursor Coefficient: 06 Hex06060606Cursor Coefficient: 28 Hex28282828TS1 EQ Control: 8D Hex8D8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4A	TSI Identifier TSI Identifier DC Balance TSI ************************************	4A 08 1E 00 00 5E 0E 00 	4A 08 1E 00 01 5E 0E 00 	4A 08 1E 00 02 5E 0E 00 	4A 4A 4A 00 03 5E 0E 00
Reset ELEOS Interval: DetassertTransmitter Preset: 0111bUse Preset: DetassertPre-Cursor Coefficient: 06 Hex06060606Cursor Coefficient: 28 Hex28282828TS1 EQ Control: 80 Hex8080808080Post-Cursor Coefficient: 0D HexReject Coefficient Values: DetassertTS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4A	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Loopback: De-assert Disable Scrambling: De-assert Compliance Receive: De-assert EQ TSI: 3A Hex EQ TSI: 3A Hex	4A 08 00 00 5E 0E 00 3A	4A 08 00 01 5E 0E 00 3A	4A 08 00 02 5E 0E 00 3A	4A 4A 00 03 5E 0E 00 00 3A
Use Preset: De-assertPre-Cursor Coefficient: 06 Hex06060606Cursor Coefficient: 28 Hex28282828TS1 EQ Control: 8D Hex8D8D8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4ATS1 Identifier4A4A4A	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Disable Link: De-assert Disable Scrambling: De-assert Compliance Receive: De-assert EQ TS1: 3A Hex Equalization Control: 10b Proceed FIFOS Literation	4A 08 1E 00 00 5E 0E 00 3A 	4A 08 00 01 5E 0E 00 3A 	4A 08 00 02 5E 0E 00 3A 	4A 4A 4A 00 3- 5E 0E 00 3A
Ose Preset: De-assertOf Use Preset: De-assertPre-Cursor Coefficient: 06 Hex060606Cursor Coefficient: 2B Hex2B2B2BTS1 EQ Control: 8D Hex8D8D8DPost-Cursor Coefficient: 0D HexReject Coefficient Values: De-assertTS1 Identifier4A4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier4ATS1 Identifier <td< td=""><td>TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Disable Scrambling: De-assert Compliance Receive: De-assert EQ TSI: 3A Hex Equalization Control: 10b Reset EIEOS Interval: De-assert Training Control: 10b</td><td>4A 08 00 00 5E 0E 00 00 3A 3A</td><td>4A 08 00 01 5E 0E 00 00 3A 3A</td><td>4A 08 00 02 5E 0E 00 00 3A 3A</td><td>4A 4A 00 3 5 5 0 0 0 3 A 3 A</td></td<>	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Disable Scrambling: De-assert Compliance Receive: De-assert EQ TSI: 3A Hex Equalization Control: 10b Reset EIEOS Interval: De-assert Training Control: 10b	4A 08 00 00 5E 0E 00 00 3A 3A	4A 08 00 01 5E 0E 00 00 3A 3A	4A 08 00 02 5E 0E 00 00 3A 3A	4A 4A 00 3 5 5 0 0 0 3 A 3 A
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Carlson Coefficient: 2D Hex2D2D2B2B2BPost-Cursor Coefficient: 0D Hex8D8D8D8DParity: AssertTS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4ATS1 Identifier4A4A4A4A	TSI Identifier TSI Identifier DC Balance TSI ************************************	4A 08 1E 00 00 5E 0E 1 00 1 1 3A 1 1 3A	4A 4A 08 1E 00 01 5E 0E 00 3A 3A	4A 08 1E 00 02 5E 0E 1 00 1 1 00 1 1 3A 1 1 1	4A 4A 5E 00
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TS1 Identifier TS1 Identifier	TSI Identifier TSI Identifier DC Balance TSI ************************************	4A 08 1E 00 00 5E 0E 1 00 1 1 3A 1 3A 1 1 3A 1 1	4A 08 1E 00 01 5E 0E 00 3A 3A 3A 	4A 08 00 02 5E 0E 00 3A 3A 3A 	4A 4A 1E 00 03 5E 00 1 1 00 1 1 1 00 1 1 1 0 0 2 8 0 1 1 1 0 0 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
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TS1 Identifier 4A 4A 4A 4A TS1 Identifier 4A 4A 4A 4A	TSI Identifier TSI Identifier DC Balance TSI Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Disable Link: De-assert Disable Scrambling: De-assert Compliance Receive: De-assert EQ TSI: 3A Hex Equalization Control: 10b Reset EIEOS Interval: De-assert Transmitter Preset: 0111b Use Preset: De-assert Pre-Cursor Coefficient: 06 Hex Cursor Coefficient: 2B Hex Post-Cursor Coefficient: 0D Hex Reject Coefficient Values: De-assert Parity: Assert TSI Identifier TSI Identifier	4A 08 1E 00 00 5E 0E 00 3A 3A 3A 3A 4A 4A	4A 4A 08 1E 00 01 5E 0E 00 3A 3A 3A 4A 4A	4A 08 1E 00 02 5E 0E 00 3A 3A 3A 3A 3A 4A 00 02 3A 4A	4A 4A 4A 1E 00 03 5E 00 1 1 00 1 1 1 00 2B 0 1 1 4A 4A
TS1 Identifier $4A$ $4A$ $4A$ $4A$	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Disable Link: De-assert Disable Scrambling: De-assert Compliance Receive: De-assert EQ TSI: 3A Hex Equalization Control: 10b Reset EIEOS Interval: De-assert Transmitter Preset: 0111b Use Preset: De-assert Pre-Cursor Coefficient: 06 Hex Cursor Coefficient: 28 Hex TSI EQ Control: 8D Hex Post-Cursor Coefficient: 00 Hex Reject Coefficient Values: De-assert Parity: Assert TSI Identifier TSI Identifier TSI Identifier	4A 4A 08 1E 00 00 5E 0E 00 3A 3A 3A 3A 4A 4A 4A 4A	4A 4A 08 1E 00 01 5E 0E 00 3A 3A 3A 3A 4A 4A 4A	4A 4A 08 1E 00 02 5E 0E 00 3A 3A 3A 3A 4A 4A 4A 4A	4AA 4A 100 003 50E
	TSI Identifier TSI Identifier DC Balance Link No: 0 Dec Lare Ordering: 0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15 N_FTS: 94 Dec Data Rate ID: 0E Hex Gen 3 rate supported Gen 1 rate supported Gen 1 rate supported Training Control: 00 Hex Hot Reset: De-assert Disable Link: De-assert Disable Link: De-assert Disable Scrambling: De-assert Compliance Receive: De-assert EQ TSI: 3A Hex Equalization Control: 10b Reset EIEOS Interval: De-assert Transmitter Preset: 0111b Use Preset: De-assert Pre-Cursor Coefficient: 06 Hex Cursor Coefficient: 28 Hex TSI EQ Control: 8D Hex Post-Cursor Coefficient: 0D Hex Reject Coefficient Values: De-assert TSI Identifier TSI Identifier TSI Identifier	4A 4A 08 1E 00 00 5E 0E 00 3A 3A 3A 4A 4A 4A 4A 4A 4A	4A 4A 08 1E 00 01 5E 0E 00 3A 3A 3A 4A 4A 4A 4A 4A	4A 4A 08 1E 00 02 5E 0E 00 3A 3A 3A 4A 4A 4A 4A 4A	4AA 4A 003 5E 0 1 00 1 1 3A 1 06 2B 0 1 4A 4A 4A

The transaction window shows the link equalization negotiation in a concise view. Because a particular training sequence may be repeated 65536 times, the transaction window allows a user to collapse these ordered sets. In this way, an entire negotiation can be viewed in a single row, reducing the need to page through thousands of rows of data.

At times, though, a platform may have a problem lane for any number of signal integrity reasons. In this case the system must provide the user access to a detailed view of the different lanes to view the link equalization negotiation. Under these circumstances, the user takes advantage of the detailed, lane by lane display in the listing window, as shown in Figure 5.

The Tektronix Logic Protocol Analyzer allows a user to view the data in a variety of correlated views. From the lowest level waveform view with correlated oscilloscope captures all the way up to a summary of the entire 16GB capture, the user can choose which views meet the needs of their application. This is especially important for PCIe3 which has blurred the lines between protocol and physical layers.

Advanced Power Management Support

The PCI Express specification contains several power saving modes. These modes are increasingly important for all types of systems. Servers are looking to cut power costs and mobile applications need to save battery life. As a result, system designers are continuously improving and optimizing the use of these power saving modes. At the same time, these modes are increasingly the source of bugs and compatibility issues. Designers and debug engineers need a tool providing visibility into these issues to take full advantage of and debug power saving modes.

At the outset of any ASPM investigation, the tool should provide a high level understanding of the system behavior. Finding out which power states are being used by which agents and how often is very simple using the LPA summary profile window. This window shows a count of all packets and ordered sets in the acquisition. The summary profile window also displays small graphs ("sparklines"), plotting the total number of each event over the time of the acquisition. Sparklines help a user understand the overall efficiency of the system or which part of a very large acquisition may be interesting to drill down into.

Figure 5. EQ Negotiation Phase 1 to Phase 2



Using the Tektronix Logic Protocol Analyzer

Figure 6 shows a summary profile window capture of a system running through L0s and L1. This indicates L0s and L1 are both occurring on both sides of the link, and that L0s is happening more frequently than L1. This is shown by the counts and timing of power management DLLPs, training sequences, fast training sequences, and electrical idle ordered sets. The viewfinder allows the user to analyze any section of the trace and jump to the first packet or ordered set of any type in that section.

Drotocol Element	In View	wfinder	In T	otal		Over		
Protocor Element	Up	Dn	Up	Dn	Max	Up	Max	Dn
 Errors 	0	0	0	0	0		0	
▶ TLPs	<u>829</u>	<u>838</u>	<u>1994</u>	<u>1577</u>	²¹⁷ W.A	www	²²³ W	prop_
▼ DLLPs	<u>991</u>	<u>1353</u>	<u>2346</u>	<u>2477</u>	¹⁹⁹ VA	m	381 🙌	
Ack	<u>630</u>	<u>545</u>	<u>1444</u>	<u>991</u>	¹⁹² N.A	www.w	¹⁸⁶ 🔨	frank
Nak	0	0	0	0	0		0	
▼ PM	<u>336</u>	<u>152</u>	<u>840</u>	<u>304</u>	⁸⁴ VM	mmm	38 🗸	fm fm
PM_Enter_L1	0	0	0	0	0		0	
PM_Enter_L23	0	0	0	0	0		0	
PM_Active_State_Request_L1	<u>336</u>	0	<u>840</u>	0	⁸⁴ VM	mmm	0	
PM_Request_Adk	0	<u>152</u>	0	<u>304</u>	0		38 🗤	fm fr
InitFC	0	0	0	0	0		0	
▶ UpdateFC	<u>25</u>	<u>656</u>	<u>62</u>	<u>1182</u>	7		¹⁹⁵ 🛝	frank
Vendor Specific	0	0	0	0	0		0	
▼ Ordered Sets	<u>1151</u>	<u>1332</u>	<u>3094</u>	<u>2939</u>	²⁵⁸ VVV	mm	²⁶³ M	
T51	<u>139</u>	<u>142</u>	<u>368</u>	<u>301</u>	35	m	⁴⁰ W	fundur_
T52	<u>228</u>	<u>228</u>	<u>593</u>	<u>490</u>	⁶⁸ WA	mm	57 W	fmm_
FTS	<u>695</u>	<u>858</u>	<u>1895</u>	<u>1924</u>	162 VVV	www.	¹⁹⁹ 📉	
EIOS	<u>43</u>	<u>51</u>	<u>116</u>	<u>113</u>	⁹ •~~	mm	¹¹ 👡	
EIEOS	0	0	0	0	0		0	
SKP	<u>46</u>	<u>53</u>	<u>122</u>	<u>111</u>	¹⁰ •~~	mm	10 🔨	
SDS	0	0	0	0	0		0	

Figure 6. Summary Window View of L0s and L1 Traffic



Using the Tektronix Logic Protocol Analyzer

Once an area of interest is identified a user can view that area in increasing levels of detail using the transaction, listing and waveform windows. Figure 7 is an example of the LPA transaction window identifying a system making very inefficient use of L1 and L0s. In this view it is easy to see which agent requested the L1, how long the system spent in L1, Recovery and L0. The system exits L1 long enough to perform one memory write. This may be necessary on this system or it may be an opportunity for optimization. The images below demonstrate the strengths of both views: the listing window reveals any lane-level issues (such as possible errors), while the transaction window provides excellent data density to rapidly navigate to areas of interest.

TLA Timestamp		Link	PacketType			Uni D	n		Uni	D Uni D	Uni D	Uni D
000:105:277	+	Upstream	PM_A	tive_State_F	Request_L1	Link (Detail	5	Dn0	Dr1	Dn2	Dn3
000:105:279	+	Upstream	PM_A	tive_State_F	Request_L1	****	FTS -	Not Aligned ****	> COM	FTS	FTS	СОМ
000:105:281	+	Downstream	PM_R	equest_Adk					FTS	FTS COM	FTS COM	FTS
000:105:294	+	Upstream	PM_A	tive_State_F	Request_L1		ETC -	Not Alagod 200	FTS	FTS	FTS	FTS
000:105:300	+	Downstream	PM_R	equest_Adk			113 -	NOC Allighed	FTS	FTS	FTS	FTS
000:105:308	+	Upstream	PM_A	tive State F	Request L1				FTS	FTS	FTS	FTS
000:105:315	+	Downstream	PM_R	PM_Request_Adk			FTS -	Not Aligned ****	> COM	FTS	FTS	COM FTS
000:105:330	+	Downstream	PM_R	equest_Adk					FTS	COM	COM	FTS
000.405-045	1	An oral of the second	-			Not A	ligned		COM	FTS	FTS	COM
000:105:345	+	Downstream	PM_R	equest_Aok		Not A	ligned		FTS	FTS	FTS	FTS
000:105:364	l+	Downstream	PM_R	equest_Aok		Align	1 ng SKP	****************	> COM	COM	COM	COM
000:105:379	÷	Downstream	PM_R	equest_Adk					SKP SKP	96 P	SKP SKP	SKP SKP
000:105:394	+	Downstream	PM_R	equest_Adk			0110.	DM Demiest Ack	SKP	SKP	SKP	SKP
000:105:413	+	Downstream	PM_R	equest_Adk		****	DLLP	PM_Request_Ack	> SOP	24	1 dia	<u></u>
000:105:428	+	Downstream	PM_R	equest_Adk			DLLP:	PM_Request_Ack	> SOP > SOP	24	00	00
000:105:443	+	Downstream	PM_R	equest_Adk		****	DLLP: DLLP:	PM_Request_Ack PM_Request_Ack	> SOP	24	80	00
000:105:458	+	Downstream	PM_R	equest_Adk			DLLP	PM_Request_Ack	> SOP	24	80	00
	80	100 001 00000000				****	DLLP	PM_Request_Ack	> SOP	24	ŏŏ	ŏŏ
000:154:448		Upstream TS	1 (16)	Width	Data Rate		DLLP	PM_Request_Ack	> SOP	24	00	00
		nk #?	1 (10)	Not Aligned	Data Data	****	DLLP: DLLP:	PM_Request_Ack PM_Request_Ack	> SOP > SOP	24	80	00
000:154:871	Li I	nk #7	1 (19)	Not Aligned	2.5/5.0		DLLP:	PM_Request_Ack	> SOP	24	00	00
	-	COLUMN SHE LICENSER	2 (22)	M.C. dab	Data Data	****	DLLP	PM_Request_Ack	> SOP	24	00	00
000:155:581		ok #0	2 (33)	vilden x16	2.5		DLLP	PM_Request_Ack	> SOP	24	00	00
	-00	156.149 Downativem	0 (00)	ALV.	Data Data		EIOS	- Not Aligned ***	> SOP > COM	COM	COM	COM
000:156:195		ownstream 15	2 (22)	width x16	2 5/5 0				IDL	IDL	IDL IDL	IDL IDL
000+157+864	+	Linstream	MWrdS	(2)	2.0/0.0	Not A	liand		IDL	IDL	IDL	IDL
000:157:963	+	Downstream	Undat	AFC.D		Not A	ligned		141	14!	14!	14!
000:157:965	÷	Downstream	Undat	AFC-ND		Not A	ligned		Unio	76 7E	IDL	Unic-
000:159:030	÷	Downstream	Ack	der conter		Not A Not A	ligned		06!	10	10	Unic- Unic-
000:150:029	F.	Downstream	Hoda	-500		Not A	ligned		EID>	37	EID>	Unk-
000:156:076	+	100 all government	Upda	leru+		Not A	ligned		No_>	No_>	COM !	No_>
	~		_			NOT A	TS1 -	Not Aligned ****	> COM!	COM!	02	No >
	_	000 150 247 Upsteem		-		Lin	k No: e Orde	unknown (Not Alig ring: Unknown (Not		00	18	COM!
000:160:817	+	Upstream	PM_A	ctive_State_F	Request_L1	N_F Dat	TS: 24 a Rate	Dec ID: 06 Hex	18	18	00 4A	03
000:160:833	+	Upstream	PM_A	ctive_State_F	Request_L1	G	en 2 r	ate supported				
000:160:853	+	Upstream	PM_A	tive_State_F	Request_L1	Tra	ining	Control: 00 Hex	00	00	4A	06

Figure 7. Transaction and Listing Window Views of L1 and L0s



Using the Tektronix Logic Protocol Analyzer

Why is the Physical Layer Important to Me?

Selecting test equipment for your PCI Express application is a very important decision. Silicon designers need to validate potential physical layer issues like power management, rate changes, or width changes. Some designers may need to margin the reference clock in order to stress test the system. Some designers need to validate with spread spectrum enabled. Other users who may not be validating the physical layer at all still need a tool that captures physical layer information when the root cause of bugs stems from the physical layer. Even users debugging higher protocol level issues like transaction latency or flow control, need test equipment supporting all of the physical layer features their system enables. In this way they can quickly identify and dispense with bugs outside their area of responsibilities.

As demonstrated in this application note, the Tektronix PCIe Logic Protocol Analyzer supports all of these features in order to enable debug all of the way from the physical layer up to the transaction layer.

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